

Digital Techniques

(Code : 22320)

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Maharashtra State Board of Technical Education (MSBTE)

**Semester III – Electronics Engineering Group,
(CO/CM/CW/DE/EJ/ET/EN/EX/EQ/IE/IS/IC/MU)**

Strictly as per new revised ‘I’ Scheme w.e.f. academic year 2018-2019

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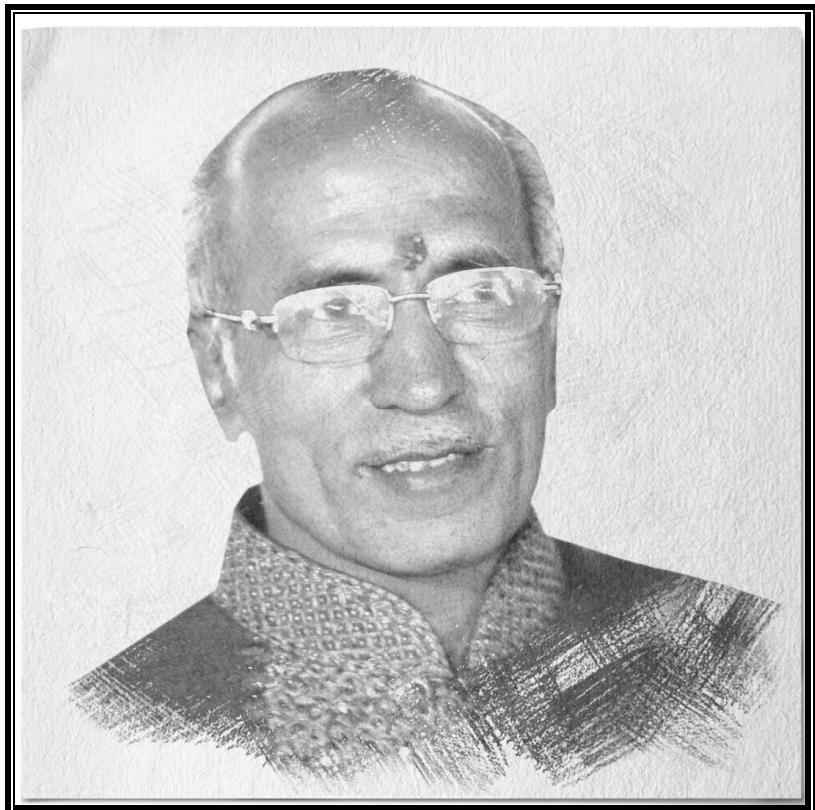
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*We dedicate this Publication soulfully and wholeheartedly,
in loving memory of our beloved founder director,
Late Shri. Pradeepji Lalchandji Lunawat,
who will always be an inspiration, a positive force and strong support
behind us.*



“My work is my prayer to God”

- Lt. Shri. Pradeepji L. Lunawat

*Soulful Tribute and Gratitude for all Your
Sacrifices, Hardwork and 40 years of Strong Vision...*

Syllabus

| Unit | Topics and Sub-topics |
|--|--|
| Unit - I : Number Systems and Codes Refer chapter 1 | 1.1 Number system : Base or radix of number system, Binary, Octal, Decimal and hexadecimal number system. 1.2 Binary arithmetic : Addition, Subtraction, Multiplication, Division. 1.3 Subtraction using 1's complement and 2's complement. 1.4 Codes : BCD, Gray code, Excess-3 and ASCII code. 1.5 BCD arithmetic : BCD addition. |
| Unit - II : Logic Gates & Logic families Refer chapters 2 and 3 | 2.1 Logic gates : Symbol, Diode/Transistor switch circuit and logical expression, Truth table of basic gates (AND, OR, NOT), Universal gates (NAND and NOR) and special purpose gates (EX-OR, EX-NOR), Tristate logic. 2.2 Boolean algebra : Laws of Boolean algebra, Duality theorem, De-Morgan's theorems. 2.3 Logic families : Characteristics of logic families : Noise margin, Power dissipation, Figure of merit, Fan-in and fan-out, Speed of operation, Comparison of TTL, CMOS, Types of TTL NAND gate. |
| Unit - III : Combinational Logic Circuits Refer chapters 4 and 5 | 3.1 Standard Boolean representation : Sum of Product (SOP) and Product of Sum (POS), Minterm and maxterm, Conversion between SOP and POS forms, Realization using NAND/NOR gates. 3.2 K-map reduction technique for the Boolean expression : Minimization of Boolean functions upto 4 variables (SOP and POS form). 3.3 Design of arithmetic circuits and code converters using K-map : Half and full adder, Half and full subtractor, Gray to binary and binary to gray (up to 4 bits). 3.4 Arithmetic circuits : (IC 7483) adder and subtractor, BCD adder. 3.5 Encoder/Decoder : Basics of encoder, Decoder, Comparison, (IC 7447) BCD to 7 segment decoder / driver. 3.6 Multiplexer and Demultiplexer : Working, Truth table and applications of multiplexers and demultiplexers, MUX tree, IC 74151 as MUX, DEMUX tree, DEMUX as decoder, IC 74155 as DEMUX. 3.7 Buffer : Tristate logic, Unidirectional and bidirectional buffer (IC74LS244, 74LS245). |

| Unit | Topics and Sub-topics |
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| Unit - V : Data Converters and PLDs Refer chapters 9, 10 and 11 | <p>5.1 Data converter : DAC : Types, Weighted resistor circuit and R-2R ladder circuit, DAC IC 0808 specifications.</p> <p>ADC : Block diagram, Types and working of dual slope ADC, SAR ADC, ADC IC 0808/0809, Specifications.</p> <p>5.2 Memory : RAM and ROM basic building blocks, Read and write operation, Types of semiconductor memories.</p> <p>5.3 PLD : Basic building blocks and types of PLDs, PLA, PAL, GAL.</p> <p>5.4 CPLD : Basic building blocks, Functionality.</p> |



**Unit-I****Chapter 1 : Number Systems and Codes 1-1 to 1-45**

Syllabus : Number system : Base or radix of number system, Binary, Octal, Decimal and hexadecimal number system, **Binary arithmetic** : Addition, Subtraction, Multiplication, Division, Subtraction using 1's complement and 2's complement. **Codes** : BCD, Gray code, Excess-3 and ASCII code. **BCD arithmetic** : BCD addition.

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Syllabus : Logic families : Characteristics of logic families : Noise margin, Power dissipation, Figure of merit, Fan-in and Fan-out, Speed of operation, Comparison of TTL, CMOS, Types of TTL NAND gate. Tristate logic.

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Multiplexer and Demultiplexer : Working, Truth table and applications of multiplexers and demultiplexers, MUX tree, IC 74151 as MUX, DEMUX tree, DEMUX as decoder, IC 74155 as DEMUX.

Buffer : Tristate logic, Unidirectional and bidirectional buffer (IC 74LS 244, 74LS245).

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Unit-IV**Chapter 6 : Flip Flops****6-1 to 6-22**

Syllabus : Basic memory cell : RS-latch using NAND and NOR, Triggering methods : Edge trigger and level trigger, **SR flip flops** : SR-flipflop, Clocked SR flip flop with preset and clear, Drawbacks of SR flip flop. **JK flip flops** : Clocked JK flip flop with preset and clear, Race around condition in JK flip flop, Master slave JK flip flop, D and T type flip flop, Excitation table of flip flops, Block schematic and function table of IC 7474, 7475.



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Unit-IV**Chapter 7 : Shift Registers****7-1 to 7-16**

Syllabus : Logic diagram of 4-bit shift register-Serial input serial output, Serial input parallel output, Parallel input serial output, Parallel input parallel output, 4 bit universal shift register, Ring counter, Twisted ring counter.

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Unit-IV**Chapter 8 : Counters** **8-1 to 8-29**

Syllabus : Asynchronous counter : 4 bit ripple counter, 4 bit up/down counter, Modulus of counter, Synchronous counter : Design of 4 bit synchronous up/down counter.

Decade counter : Block schematic of IC 7490 decade counter, IC 7490 as MOD N counter, Ring counter, Twisted ring counter.

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Unit-V

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| Chapter 9 : A-D and D-A Converters | 9-1 to 9-23 |
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Syllabus : Data converter : DAC : Types, Weighted resistor circuit and R-2R ladder circuit, DAC IC 0808 specifications.

ADC : Block diagram, Types and working of dual slope ADC, SAR ADC, ADC IC 0808/0809, Specifications.

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**Unit-V****Chapter 10 : Memories 10-1 to 10-16**

Syllabus : Memory : RAM and ROM basic building blocks, Read and write operation, Types of semiconductor memories.

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Unit-V**Chapter 11 : Programmable Logic Devices 11-1 to 11-15**

Syllabus : PLD : Basic building blocks and types of PLDs, PLA, PAL, GAL. CPLD : Basic building blocks, Functionality.

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